WHAT IS CLAIMED IS:

1. A semiconductor component comprising:

a base die comprising a substrate having a back side, and a plurality of conductive vias in the substrate;

a secondary die having a circuit side bonded to the back side and a plurality of contacts bonded to the conductive vias; and

a plurality of terminal contacts on the base die in electrical communication with the conductive vias.

2. The semiconductor component of claim 1 further comprising an encapsulant on the back side at least partially encapsulating the secondary die.

3. The semiconductor component of claim 1 further comprising a polymer layer on the base die configured as a protective member, a rigidifying member and a stencil for forming the terminal contacts.

4. The semiconductor component of claim 1 further comprising a second secondary die bonded to the secondary die.

5. The semiconductor component of claim 1 the base die and the secondary die comprise thinned dice.

6. The semiconductor component of claim 1 wherein the conductive vias comprise openings in the substrate at least partially filled with a conductive material.

7. A semiconductor component comprising:

a thinned base die comprising a circuit side, a back side, a plurality of conductive vias and a plurality of

contacts on the back side in electrical communication with the conductive vias;

a thinned secondary die stacked on the base die and bonded to the contacts; and

a plurality of terminal contacts on the circuit side in electrical communication with the conductive vias.

8. The semiconductor component of claim 7 further comprising an encapsulant on the back side at least partially encapsulating the secondary die.

9. The semiconductor component of claim 7 further comprising a cap plate bonded to the secondary die comprising a plurality of conductors configured to electrically connect selected base die contacts to selected secondary die contacts.

10. The semiconductor component of claim 7 further comprising a cap plate bonded to the secondary die and a plurality of electrical components on the cap plate in electrical communication with the secondary die.

11. The semiconductor component of claim 7 wherein the contacts comprise bumps in physical contact with the conductive vias.

12. The semiconductor component of claim 7 wherein a peripheral outline of the base die matches that of the component.

13. The semiconductor component of claim 7 wherein the conductive vias comprise a metal and a solder alloy.

14. A semiconductor component comprising:

a base die comprising a thinned semiconductor substrate and a plurality of conductors on the substrate;

an internal signal transmission system comprising a plurality of conductive vias in the substrate in electrical communication with the conductors, and a plurality of contacts on the conductive vias;

a secondary die bonded to the contacts; and

a plurality of terminal contacts on the conductors.

15. The semiconductor component of claim 14 wherein the secondary die comprises a plurality of metal bumps bonded to the contacts.

16. The semiconductor component of claim 14 wherein the conductors comprise redistribution conductors on a circuit side of the base die.

17. The semiconductor component of claim 14 further comprising a cap plate bonded to the secondary die and a plurality of electrical components on the cap plate in electrical communication with the secondary die.

18. The semiconductor component of claim 14 further comprising a cap plate bonded to the secondary die configured to short selected contacts on the base die to selected contacts on the secondary die.

19. The semiconductor component of claim 14 further comprising an electrically conductive polymer bonding the secondary die to the contacts.

20. The semiconductor component of claim 14 further comprising a module substrate bonded to the base die.

21. The semiconductor component of claim 14 wherein the secondary die and the substrate have a thickness of about 100 μm to 600 μm.

22. The semiconductor component of claim 14 wherein the conductive vias comprise openings in the substrate at least partially filled with a material selected from the group consisting of metal, solder, conductive polymers and nano-particle conductive polymers.

23. A semiconductor component comprising:

a base die comprising a thinned semiconductor substrate having a peripheral outline, a circuit side, a back side, and a plurality of conductive vias in the substrate;

a thinned secondary die bonded to the back side and comprising a plurality of integrated circuits in electrical communication with the conductive vias;

an encapsulant on the back side having the peripheral outline and at least partially encapsulating the secondary die;

a polymer layer on the circuit side having the peripheral outline and configured as a protective and rigidifying member for the component; and

a plurality of terminal contacts on the circuit side in electrical communication with the conductive vias.

24. The semiconductor component of claim 23 wherein the polymer layer is configured as a stencil for forming the terminal contacts.

25. The semiconductor component of claim 23 wherein the secondary die comprises a plurality of bumped contacts bonded to the conductive vias.

26. The semiconductor component of claim 23 wherein the base die comprises a plurality of bumped contacts on the conductive vias bonded to the secondary die.

27. The semiconductor component of claim 23 further comprising a second secondary die bonded to the thinned secondary die in electrical communication with the conductive vias.

28. A semiconductor component comprising:

a first base die comprising a plurality of first conductive vias;

a second base die stacked and bonded to the first base die comprising a plurality of second conductive vias in electrical communication with the first conductive vias;

a secondary die stacked and bonded to the second base die comprising a plurality of bumped contacts bonded to the second conductive vias; and

a plurality of terminal contacts on the first base die in electrical communication with the first conductive vias.

29. The semiconductor component of claim 28 wherein the terminal contacts comprise balls or bumps in a grid array.

30. The semiconductor component of claim 28 further comprising an underfill layer between the first base die and the secondary die.

31. The semiconductor component of claim 28 wherein the first base die, the second base die and the secondary die comprise known good dice.

32. The semiconductor component of claim 28 wherein the secondary die comprises a cap plate having a plurality of electrical components thereon.

33. The semiconductor component of claim 28 wherein the first conductive vias and the second conductive vias comprise a material selected from the group consisting of metal, solder, conductive polymers and nano-particle conductive polymers.

34. The semiconductor component of claim 28 wherein the bumped contacts comprise metal bumps in physical contact with the conductive vias.

35. A semiconductor component comprising:

a base die comprising a semiconductor substrate having a circuit side and a back side, a plurality of die contacts on the circuit side, a plurality of conductive vias in the substrate in electrical communication with the die contacts, a plurality of redistribution conductors on the circuit side in electrical communication with the conductive vias, and a plurality of terminal contacts on the circuit side in electrical communication with the conductors;

a secondary die bonded to the back side;

an underfill layer bonding the secondary die to the base die; and

a plurality of bumped contacts bonded to the conductive vias and to the secondary die.

36. The semiconductor component of claim 35 further comprising a polymer layer on the circuit side configured as a rigidifying member, a protective member, and a stencil for forming the terminal contacts.

37. The semiconductor component of claim 35 further comprising a module substrate bonded to the base die.

38. The semiconductor component of claim 35 further comprising an encapsulant on the back side at least partially encapsulating the secondary die.

39. The semiconductor component of claim 35 further comprising an electrically insulating polymer layer in the conductive vias and on the back side.

40. The semiconductor component of claim 35 wherein the base die and the secondary die comprise thinned dice.

41. The semiconductor component of claim 35 wherein the terminal contacts comprise bumps, balls or pins in a grid array.

42. The semiconductor component of claim 35 wherein the conductive vias comprise lasered openings and a conductive material in the openings, and the bumped contacts comprise solder bumps bonded to the conductive material.

43. The semiconductor component of claim 35 wherein the base die and the component have a same peripheral outline.

44. The semiconductor component of claim 35 wherein the conductive vias comprise openings in the substrate, an insulating layer on the openings, and a conductive material in the openings.

45. A semiconductor component comprising:

a base die comprising a circuit side, a back side, a plurality of conductive vias and a plurality of contacts on the back side in electrical communication with the conductive vias;

a first secondary die stacked on the base die and bonded to the contacts, the first secondary die comprising a plurality of secondary conductive vias and a plurality of secondary contacts in electrical communication with the secondary conductive vias;

a second secondary die stacked on the first secondary die and bonded to the secondary contacts; and

a plurality of terminal contacts on the circuit side in electrical communication with the conductive vias.

46. The semiconductor component of claim 45 further comprising an encapsulant on the back side at least partially encapsulating the first secondary die and the second secondary die.

47. The semiconductor component of claim 45 further comprising a polymer layer on the circuit side configured as a rigidifying member, a protective member, and a stencil for forming the terminal contacts.

48. The semiconductor component of claim 45 wherein the base die, the first secondary die and the second secondary die comprise thinned dice.

49. The semiconductor component of claim 45 wherein the second secondary die includes a plurality of electrical components thereon in electrical communication with the secondary contacts.

50. The semiconductor component of claim 45 wherein the contacts comprise bumps in physical contact with the conductive vias.

51. A method for fabricating a semiconductor component comprising:

providing a base die comprising a substrate having a back side;

forming a plurality of conductive vias in the substrate;

providing a secondary die comprising a circuit side and a plurality of contacts;

bonding the secondary die to the back side and the contacts to the conductive vias; and

forming a plurality of terminal contacts on the base die in electrical communication with the conductive vias.

52. The method of claim 51 further comprising prior to the bonding step thinning the base die, and following the bonding step thinning the secondary die.

53. The method of claim 51 further comprising forming a polymer layer on the base die proximate to the terminal contacts configured to protect and rigidify the component.

54. The method of claim 51 wherein the forming the conductive vias step comprises laser machining openings from the back side into the substrate, forming insulating layers in the openings and depositing a conductive material in the openings.

55. The method of claim 51 wherein the forming the conductive vias step comprises forming openings in the substrate depositing a metal in the openings and then squeegeeing a solder into the openings.

56. A method for fabricating a semiconductor component comprising:

providing a base die comprising a circuit side, a back side, a semiconductor substrate and a plurality of conductive vias in the substrate;

providing a secondary die comprising a plurality of contacts;

bonding the secondary die to the back side and the contacts to the conductive vias; and

forming a plurality of terminal contacts on the circuit side in electrical communication with the conductive vias.

57. The method of claim 56 further comprising forming an encapsulant on the back side at least partially encapsulating the secondary die.

58. The method of claim 56 wherein the base die is contained on a base wafer containing a plurality of base dice and the bonding step is performed by placing a plurality of secondary dice on the base dice.

59. The method of claim 56 wherein the base die is contained on a base wafer containing a plurality of base dice, the secondary die is contained on a secondary wafer containing a plurality of secondary dice and the bonding step is performed by bonding the base wafer to the secondary wafer.

60. The method of claim 56 further comprising forming a polymer layer on the circuit side configured as a stencil for forming the terminal contacts.

61. The method of claim 56 wherein the base die and the secondary die comprise thinned dice.

62. A method for fabricating a semiconductor component comprising:

providing base die on a base wafer;

forming a plurality of conductive vias on the base die;

providing a secondary die comprising a plurality of contacts;

bonding the secondary die to the base die with the contacts in electrical communication with the conductive vias;

thinning the secondary die while bonded to the base die on the wafer;

forming a plurality of terminal contacts on the base die in electrical communication with the conductive vias; and

singulating the base die with the secondary die bonded thereto from the wafer.

63. The method of claim 62 further comprising thinning the base die on the base wafer prior to the bonding step.

64. The method of claim 62 wherein the forming the conductive vias step comprises forming openings in the base die and at least partially filling the openings with a metal a conductive polymer, or a nano particle conductive polymer.

65. The of claim 62 further comprising testing the secondary die and the base die prior to the bonding step.

66. The method of claim 62 further comprising following the singulating step mounting the base die to a module substrate.

67. The method of claim 62 wherein the secondary die is contained on a secondary wafer and the bonding step is performed by bonding the secondary wafer to the base wafer.

68. A method for fabricating a semiconductor component comprising:

providing a tested singulated secondary die comprising a plurality of bumped contacts;

providing a wafer comprising a base die comprising a substrate having a circuit side and a back side, a plurality of integrated circuits in the substrate, and a plurality of contacts on the substrate in electrical communication with the integrated circuits;

forming a polymer layer on the circuit side having openings aligned with the contacts;

forming a plurality of conductive vias in the back side extending through the substrate to the contacts;

bonding the secondary die to the back side with the bumped contacts in electrical communication with the conductive vias; and

forming terminal contacts in the openings using the polymer layer as a stencil.

69. The method of claim 68 wherein the forming the polymer layer step is performed using a laser imaging process.

70. The method of claim 68 wherein the laser imaging process comprises heat curing or UV curing the polymer layer.

71. The method of claim 68 wherein the forming the polymer layer step comprises depositing and curing a polymer material.

72. The method of claim 68 wherein the forming the polymer layer step is performed using a photo lithography process.

73. The method of claim 68 wherein the forming the conductive vias step comprises laser machining and thinning the base die.

74. The method of claim 68 further comprising following the bonding step, thinning the secondary die by grinding, polishing, or etching the secondary die.

75. A method for fabricating a semiconductor component comprising:

providing a base die comprising a substrate having a back side;

forming a plurality of conductive vias in the substrate;

providing a first secondary die comprising a circuit side, a plurality of contacts and a plurality of secondary conductive vias;

bonding the secondary die to the back side and the contacts to the conductive vias;

providing a second secondary die; and

bonding the second secondary die to the first secondary die in electrical communication with the secondary conductive vias.

76. The method of claim 75 further comprising forming a plurality of terminal contacts on the base die in electrical communication with the conductive vias.

77. The method of claim 75 further comprising thinning the first secondary die, the second secondary die and the base die.

78. The method of claim 75 wherein the forming the conductive vias step comprises laser machining openings in the substrate and then depositing a nano particle conductive polymer in the openings.

79. The method of claim 75 further comprising forming a polymer layer on the base die configured to protect and rigidify the component.

80. A system comprising:

a substrate; and

a semiconductor component on the substrate comprising a base die comprising a substrate having a back side, and a plurality of conductive vias in the substrate, a secondary die having a circuit side bonded to the back side and a plurality of contacts bonded to the conductive vias, and a plurality of terminal contacts on the base die in electrical communication with the conductive vias.

81. The system of claim 80 further comprising a cap plate bonded to the secondary die configured to short selected contacts on the base die to selected contacts on the secondary die.

81. The system of claim 80 further comprising a cap plate bonded to the secondary die and at least one electrical element on the cap plate in electrical communication with the secondary die.

83. The system of claim 80 wherein the substrate is contained in a device selected from the group consisting of a module, a package, a computer, a camcorder, a camera, a cell phone, and a medical device.

84. The system of claim 80 further comprising an encapsulant on the back side at least partially encapsulating the secondary die.

85. The system of claim 80 further comprising a polymer layer on the base die configured as a protective member, a rigidifying member and a stencil for forming the terminal contacts.

86. A system comprising:

a substrate comprising a plurality of electrodes; and

a semiconductor component on the substrate comprising:

a thinned base die comprising a circuit side, a back side, a plurality of conductive vias and a plurality of contacts on the back side in electrical communication with the conductive vias;

a thinned secondary die stacked on the base die and bonded to the contacts; and

a plurality of terminal contacts on the circuit side in electrical communication with the conductive vias and bonded to the electrodes.

87. The system of claim 86 further comprising a second secondary die stacked on and bonded to the secondary die.

88. The system of claim 86 further comprising a cap plate stacked on and bonded to the secondary die.

89. The system of claim 86 wherein the system comprises a multi chip module, a system in a package, a computer, a camcorder, a camera, a cell phone, or a medical device.

90. A system comprising:

a substrate comprising a plurality of electrodes;

a semiconductor component on the substrate comprising:

a base die comprising a thinned substrate having a peripheral outline and a plurality of conductive vias in the substrate;

a thinned secondary die comprising a plurality of bumped contacts bonded to the conductive vias and electrically connecting the base die and the secondary die;

an encapsulant on the base die having the peripheral outline and at least partially encapsulating the secondary die;

a rigidifying polymer layer on the base die having the peripheral outline; and

a plurality of terminal contacts on the base die proximate to the polymer layer in electrical communication with the conductive vias and bonded to the electrodes.

91. The system of claim 90 wherein the substrate comprises a module substrate or a package substrate.

92. The system of claim 90 wherein the conductive vias comprise a material selected from the group consisting

of metal, solder, conductive polymers and nano particle conductive polymers.

93. The system of claim 90 further comprising a plurality of components on the substrate substantially identical to the component.

94. The system of claim 90 wherein the polymer layer comprises a stencil for forming the terminal contacts.

95. The system of claim 90 wherein the conductive vias comprise openings in the substrate, an insulating layer on the openings, and a conductive material in the openings.

96. The system of claim 90 further comprising a second secondary die stacked on and bonded to the secondary die.

97. The system of claim 90 further comprising a cap plate stacked on and bonded to the secondary die.

98. The system of claim 90 further comprising a cap plate stacked on and bonded to the secondary die and configured to short selected contacts on the base die to selected contacts on the secondary die.

99. The system of claim 90 further comprising a cap plate stacked on and bonded to the secondary die and a plurality of electrical components on the cap plate in electrical communication with the secondary die.

100. The system of claim 90 wherein the system comprises a multi chip module, a system in a package, a computer, a camcorder, a camera, a cell phone, or a medical device.